R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 7 lines 11-14, page 10 lines 8-13, page 11 line 9 thru page 12 line 2, page 13 lines 5-12, page 14 line 3 thru page 15 line 6, page 15 lines 14-21, page 16 lines 5-19 and FIGS. 2-5 as originally filed. Thus, no new matter has been added.

IN THE DRAWINGS

Applicants' representative respectfully traverses the request to label FIG. 1 as prior art. No admission has been made regarding FIG. 1 as prior art and the request should be withdrawn. After the Examiner withdraws the rejection over the background section, Applicants' representative will label FIG. 1 as "conventional".

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 4, 5 and 13 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-3 and 6-16 under 35 U.S.C. §103 as being unpatentable over the Background Section of the present application (hereafter Background Section) in view of Jin '464 and Levitt '186 has been obviated by appropriate amendment and should be withdrawn.

Jin concerns a high speed boundary scan design (Title). Levitt concerns a method and apparatus for interconnecting testing without speed degradation (Title). Applicant's representative respectfully traverses the assertion on page 2, section 1 of the Office Action that the Background Section and FIG. 1 of the present application qualify as prior art under 35 U.S.C. §102/103. No such admission has been made. Therefore, *prima facie* obviousness has not been established and the rejection should be withdrawn.

Claim 1 provides a first pad circuit configured to transfer a first data signal in response to a pad control signal and a second pad circuit configured to generate a second data signal from an input signal in response to the pad control signal. In contrast, each of the Background Section, Jin and Levitt appear to be silent regarding two pad circuits operating in response to a control signal. Therefore, the Background Section, Jin and Levitt, alone or in combination, do not appear to teach or suggest a first pad circuit configured to transfer a first data signal in response to a pad control signal and a second pad circuit configured to

generate a second data signal from an input signal in response to the pad control signal as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 9 provides a step for measuring a response of a pad circuit based upon a test data signal. In contrast, the Background Section, Jin and Levitt each appear to be silent regarding response measurements based upon test data in a boundary scan chain. Therefore, the Background Section, Jin and Levitt, alone or in combination, do not appear to teach or suggest a step for measuring a response of a pad circuit based upon a test data signal. Claim 16 provides language similar to claim 9. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides a test circuit configured to clock a test data signal at a predetermined time to cause a first pad circuit to under go a predetermined state transition for a transition response measurement of the first pad circuit. As noted above, each of the Background Section, Jin and Levitt appear to be silent regarding transition response measurements. Therefore, the Background Section, Jin and Levitt, alone or in combination, do not appear to teach or suggest a test circuit configured to clock a test data signal at a predetermined time to cause a first pad circuit to undergo a predetermined state transition for a

transition response measurement of the first pad circuit as presently claimed. Claim 5 provides language similar to claim 3. As such, claims 3 and 5 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 11 provides a step for measuring a transition response of a pad circuit based upon a test data signal for driving an output signal. In contrast, the Background Section, Jin and Levitt each appear to be silent regarding transition response measurements for output signals. Therefore, the Background Section, Jin and Levitt, alone or in combination, do not appear to teach or suggest a step for measuring a transition response of a pad circuit based upon a test data signal for driving an output signal as presently claimed. Claim 14 provides language similar to claim 11. As such, claims 11 and 14 are fully patentable over the cited references and the rejection should be withdrawn.

The Office Action has not provided clear and particular evidence of motivation to combine the references. Regarding the combination of the Background Section and Jin, the assertion that "the storage circuitry allows for properly coordinated JTAG control signal to be applied thus allowing for tight control of the boundary scan testing process" does not appear in the cited text of Jin in column 7, lines 23-43. As such, the first asserted motivation appears to be merely a conclusory statement. Regarding motivation to add Levitt, the assertion on page 4 of the Office

Action that "it allows for both external and internal control of the testing circuitry" does not appear to exist in the cited text of Levitt in column 2, lines 40-67. As such, the second asserted motivation to combine appears to be merely a conclusory statement. Furthermore, no admission of prior art has been made regarding the Background Section or FIG. 1 of the present application. Therefore, *prima facie* obviousness has not been established for lack of clear and particular motivation to combine the references. The Examiner is respectfully requested to either (1) provide clear and concise cites to Jin and Levitt for the asserted motivation to combine the references or (2) withdrawn the rejection.

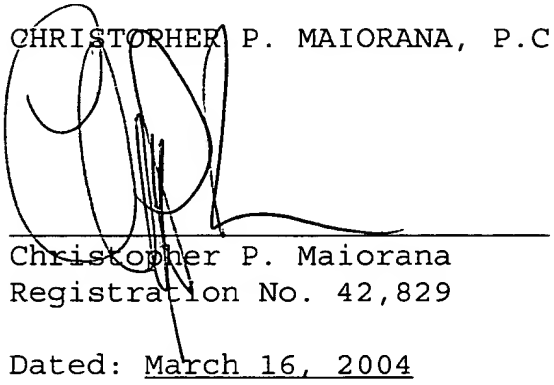
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829

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c/o Peter R. Scott
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035
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